MSLIN98-002C
Serial Number 09/251,183

IN THE CLAIMS

Please amend the claims as follows.

1. A method for forming a top metallization system for high performance integrated circuits, comprising:

forming an integrated circuit containing a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and containing a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metallization structure;

depositing an insulating, separating layer <u>of polymer</u> over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said <u>polymer</u> insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metallization structure;

depositing metal contacts in said openings; and

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system contains a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

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14. Please cancel claim 14.

15. The method of claim 1 wherein said insulating, separating of polymer layers contains polyimide.

8 ~~16~~. The method of claim 1 wherein said insulating, separating layer of polymer contains polymer benzocyclobutene (BCB).

B2

9 ~~17~~. The method of claim 1 wherein said polymer insulating, separating layer is of a thickness after curing within a range of approximately 1.0 to 30 um.

B2

10 ~~18~~. The method of claim 1 wherein said polymer insulating, separating layer is spin-on coated and cured.

B3

19. The method of claim 1 wherein said polymer insulating, separating layers after said spin-on coating are cured at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours said curing to occur within a vacuum or nitrogen ambient.

B4

12 ~~20~~. The method of claim 8 ~~16~~ wherein said polymer insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.

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21. The method of claim 20 wherein one or more of said one or more polymer insulating, separating layers after each process step of said spin on coating are cured at a temperature within a range of approximately 250 to 450 degrees C. for a time within a range of approximately 0.5 to 1.5 hours said curing to occur within a vacuum or nitrogen ambient.

21 ~~49~~. A method for forming a top metallization system for high performance integrated circuits, comprising:

forming an integrated circuit containing a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and containing a plurality of first metal lines;

depositing [an] a polymer insulating, separating layer over said semiconductor substrate;

forming openings through said polymer insulating, separating layer to expose upper metal portions of said interconnecting metallization structure;

depositing metal contacts in said openings; and

forming said top metallization system connected to said interconnecting metallization structure, wherein said top metallization system contains a plurality of top metal lines, in one or more layers, having a width substantially greater than said first metal lines.

61. Please cancel claim 61.

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28 ~~62~~. The method of claim ~~49~~ 24 wherein said polymer insulating, separating layer is selected from the group containing polyimide and benzocyclobutene (BCB).

29 ~~63~~. A method for forming a top metallization system for high performance integrated circuits, comprising: forming an integrated circuit containing a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and containing a plurality of fine-wire metal lines;
depositing a passivation layer over said interconnecting fine-wire metallization structure;
depositing [an] a polymer insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;
forming openings through said polymer insulating, separating layer to expose upper metal portions of said overlaying interconnecting metallization structure;
depositing metal contacts in said openings thereby raising a plurality of contact points in said overlaying interconnecting metallization structure to a top surface of said polymer

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B4 cont'd.

insulating, separating layer thereby creating elevated interconnecting metallization contact points;

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system contains a plurality of top wide-metal lines, in one or more layers, having a width substantially greater than said fine-wire metal lines, wherein said top metallization system directly interconnects said elevated interconnecting metallization contact points thereby functionally extending or connecting said fine-wire metal interconnects with said wide-wire metal interconnects thereby furthermore establishing electrical interconnects between multiple points within said fine-wire interconnects.

69. Please cancel claim 69.

B8

~~70~~ 35. The method of claim ~~63~~ 29 wherein said polymer insulating, separating layer contains polyimide.

~~71~~ 34. The method of claim ~~63~~ 29 wherein said polymer insulating, separating layer contains the polymer benzocyclobutene (BCB).

37 ~~72~~. The method of claim 29 ~~63~~ wherein said polymer insulating, separating layer is of a thickness after curing within a range of approximately 1.0 to 30 um.

B8 cont'd

38 ~~73~~. The method of claim 29 ~~63~~ wherein said polymer insulating, separating layer is spin-on coated and cured.

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41 ~~76~~. The method of claim 29 ~~63~~ wherein said openings through said polymer insulating, separating layer have sloping sides and wherein each of said openings is wider at its top.

B10

Please add the following new claims.

sub D8

B11

81. A method for forming a top metallization system for high performance integrated circuits comprising:
forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines in one or more layers, wherein intermetal dielectric layers are formed between said plurality of first metal lines;
depositing a passivation layer over said interconnecting metallization structure;

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depositing a polymer insulating, separating layer over said passivation layer that is substantially thicker than each of raid intermetal dielectric layers;

forming openings through said polymer insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metallization structure;

depositing metal contacts in said openings; and

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

82. The method of Claim 81 wherein said top metallization system further comprises one or more layers of metal whereby each layer of metal is separated from adjacent layers of metal by thick insulator layers of polymer, and wherein said thick insulator layers of polyimide are substantially thicker than said intermetal dielectric layers.

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~~83~~. A method for forming a top metallization system for high performance integrated circuits comprising:

forming an integrated circuit comprising a plurality of devices

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formed in and on a semiconductor substrate, with an overlaying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines in one or more layers, wherein intermetal dielectric layers are formed between said plurality of first metal lines;

depositing a passivation layer over said interconnecting metallization structure;

depositing a polymer insulating, separating layer over said passivation layer that is substantially thicker than each of said intermetal dielectric layers;

B11 Con'd.

forming openings through said polymer insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metallization structure;

depositing metal contacts in said openings; and

forming said top metallization system connected to said overlaying interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a thickness substantially greater than said first metal lines.

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b

IN THE DRAWINGS

The drawings have been amended as kindly suggested by Examiner, a copy of the updated drawings is attached.

REMARKS

Claim rejections - 37 CFR 1.75 (c)

Examiner Garcia is thanked for thoroughly examining the subject Patent Application. All claims are now considered to be in condition for allowance.

The invention teaches a method for forming a top level of metal interconnects for high performance integrated. The process of the invention starts with a semiconductor substrate, semiconductor devices with points of electrical contact have been formed in or on the surface of the substrate. A layer of electrical interconnecting metallization that contains metal lines, contact points and vias is created over surface of the substrate. A layer of passivation is deposited over the layer of interconnecting metallization over which a thick insulating, separating layer of polymer is deposited. Openings are formed through the layer of polymer and the passivation layer to expose

upper metal portions of the overlaying interconnecting metallization structure. Metal contacts are deposited in the openings and a top metallization system is formed on the surface of the layer of polymer that is connected to the interconnecting metallization structure. The top metallization system contains metal lines, in one or more layers, these metal lines have a width substantially greater than the metal lines contained in the layer of electrical interconnecting metallization that has been provided close to the surface of the substrate.

Reconsideration of the rejection of Claims 1-28 and 49-79 as being rejected under 36 U.S.C. 103 as being unpatentable over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Woff and Cronin, is respectfully requested, in light of the following.

The subject claims have been amended to more clearly describe the invention, by adding the material, polymer, used for the insulating, separating layer. The purpose of this thick layer of polymer is to allow for redistribution of the fine wires of the interconnect network that has been created over the surface of the substrate and layer of interconnect wires that are created on the surface of the layer of polymer. The functions of the fine wires that have been created close to the

surface of the substrate is supplemented by the functions of the more robust wires that are created on the surface of the thick layer of polymer. The thick layer of polymer allows for the creation of interconnect lines that are thicker and can be made in a less stringent processing environment, allowing for a semiconductor package that considerably extends the packaging capabilities of the underlying semiconductor devices. This organic layer of polymer is formed above the passivation layer 4 since the polymer layer 6 could be a source of ion contamination which could affect the underlying devices. The passivation layer 4, as is well known in the art, is a continuous layer overlaying the entire lower fine-line metallization system and devices, and protects the lower structures from both ion contaminants and moisture.

Bandyopadhyay, either alone or in combination with the other references cited above, fails to disclose or render obvious the subject claimed invention. Bandyopadhyay does not teach or suggest the formation of a polymer insulating, separating layer over a passivation layer. The examiner characterizes layer 22 of Bandyopadhyay as a passivation layer, and layer 24 as an insulating, separating layer that is substantially thicker than the passivation layer. However, layer 22 is not a passivation layer, which as known in the art is used

only after the completion of all fine-line metallization, to avoid ion and environmental contamination, as noted above.

It can be seen in Fig. 2 of Bandyopadhyay that further metal layers 14 and 16 are formed above layer 22. Layer 22 is therefore not a passivation layer, as known in the art, but rather an intermetal dielectric (see col. 5, lines 26-33). Furthermore, layer 24 of Bandyopadhyay is not a polymer (which is an organic material) separating, insulating layer but rather an inorganic intermetal dielectric. An organic polymer could not be used at layer 24 of Bandyopadhyay as it would be a source of ion contaminants and could not be used in the absence of an underlying passivation layer. If an organic polymer were used for layer 24, and a passivation layer also used, the passivation layer would be formed well above layer 24, after completion of the metallization system, and thus would not protect the devices of Bandyopadhyay from polymer-originated contamination.

The Examiner states in the final office action that Bandyopadhyay is relied upon for the purpose of disclosing the use of PECVD nitride - PECVD oxide as the passivation layer. There is no disclosure or suggestion in Bandyopadhyay of any passivation layer, much less materials or deposition processes that would be used for such a layer. Bandyopadhyay does disclose

the use of a nitride for element 28 (see Fig. 2), however this element is an etch stop and is patterned (see col. 6, lines 6-24). Etch stop 28 could not be used for passivation since a passivation layer must be continuous and completely overlying the lower layers that are to be protected, as is known in the art and described above.

Furthermore, Bandyopadhyay's etch stop element 28 is not used in the subject claimed invention, which has a polymer insulating, separating layer 6 formed over a passivation layer 4, with no intervening layers such as etch stops. Such an etch stop would serve no purpose in the subject invention, since contact must be made to contact pads 6 which lie under the passivation layer 4 (see Fig. 1 of the subject application), and not to any etch stop elements which in Bandyopadhyay are on top of the dielectric 22.

The Examiner also states in the final office action that Bandyopadhyay is relied upon for the purpose of disclosing a thick layer of polymer or BCB used as an insulating layer in the upper level of the metal interconnect system of the invention. However, it appears that Bandyopadhyay fails to disclose the use of any polymer materials. The Examiner is asked to specifically

point out where in the subject patent these materials or concepts are discussed.

These arguments are further augmented by the observation that, in Yamada '778 the layer of nitride is used as an etch stop whereas, in the instant invention, the layer of nitride is used as part of and as a continuous layer of passivation. This is a significant difference in both the functionality of the layer of nitride during the processing sequence of the instant invention as opposed to Yamada '778 and in the manner in which the layer of nitride is used as part of the present invention. An etch stop layer serves the function of stopping a process of etch from proceeding through the etch stop layer and as such protects underlying layers from being affected by the etch. The layer of nitride of the instant invention serves the function of extending the function of the passivation layer that is deposited over the surface of the lower fine-level metallization. This extension allows for the creation of interconnect metal lines to be created in the layer of nitride, a function that is differs significantly from the function of serving as an etch stop layer. Figs. 1 and 2 of the instant invention clearly highlight this difference in indicating (fine wire) metal lines that are distributed throughout the layers 3 of the layer of nitride. A layer of passivation must, as is

known in the art, be a continuous layer. Layer 22 as used by Bandyopadhyay et al. is not a layer of passivation but a layer of dielectric. A typical layer of passivation is applied to prevent ion penetration or to protect a semiconductor surface against damage caused by the environment (surface scratching and the like) or to protect a semiconductor surface against moisture penetration. The layer of passivation that is used by the present invention (layer 4, Fig. 1) serves all these purposes. In addition, the functional use of this layer of passivation of the invention is further extended by the underlying layer of nitride that allows for the creation of interconnect metal liners in the layer of nitride, further expanding fine wiring capability close to the surface of the underlying substrate.

In addition, as noted above, Bandyopadhyay et al. do not disclose a thick layer of polymer. Key to the present invention is the use of a thick layer of polymer, the importance of the thickness of the layer of polymer has clearly been emphasized throughout the specifications. Bandyopadhyay et al. do not disclose that the insulating, separating layer 24 is substantially thicker than passivation layer 22 (Fig. 2). The layer of polymer of the present invention is (required to be) thick in view of the fact that the present invention allows for the creation of thick layer of metal on the surface of the layer

of polymer. In the case of Bandyopadhyay et al., no nitride layer is provided under layer 24, the nitride that is provided in the present invention underlying the layer of thick polymer is required to prevent ion contamination from the polymer into underlying surfaces. Since Bandyopadhyay et al. do not provide for this layer of nitride, Bandyopadhyay et al. cannot use a layer of polymer since this layer of polymer would cause, without the layer of nitride, unacceptable ion diffusion. If Bandyopadhyay et al. do apply nitride, this application will be above layer 24, Fig. 2, and will therefore not have the same function or effect as the layer of nitride of the present invention.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of Claims 1-28 and 49-79 under 35 U.S.C. as being unpatentable over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin be withdrawn.

Claims 3-10 and 50-55 are objected to under 37 CFR 1.75 (c) as being improper dependent form for failing to further limit the subject matter of previous claim. Reconsideration of rejection of claims 3-10 and 50-55 under 37 CFR 1.75 (c) is respectfully requested based on the following arguments.

For each of the claims 3-10 and 50-55 the claim further and in detail specifies the application of the top metallization system and the nature of the construction of the top metallization system with respect to the underlying interconnect metallization structure. For instance, in claim 3, the claim specifies that the metallization system of the invention can be used for the creation of signal lines whereby these signal lines are created such that these lines can be significantly wider than the interconnect lines of the underlying interconnecting metallization structure. This claim therefore claims that the metal lines that form the top metallization system can be used for signal lines (thereby providing a very specific function to the lines of the top metallization system) while claim 3 further specifies that these signal lines can meet specific electrical function of (signal line) interconnect by allowing for metal lines (in the top metallization system of the invention) that are wide when compared with the metal lines of the underlying interconnect network. This combination of signal lines plus the potential for creating wider signal lines is a key aspect of the present invention whereby this key aspect of the present invention is provided by the specific creation of the top metallization system as detailed in the specification of the invention.

The specific comments that have been provided relative to claim 3 equally apply to all the other claims within the group of claims 3-10 and 50-55. For each of the claims within this group of claims, the claim in question specifies a characteristic of the top metallization system of the invention that is provided by following the processes of the invention, these characteristics of the metallization system of the invention are unique to the invention are therefore claimed as such. The claims that rare contained within claims 3-10 and 50-55 claim particular uses of the metal interconnects that are formed as part of the top metallization system of the invention such as signal lines, power planes, ground buses and combinations thereof and, where required, further claim aspects of construction of the metal interconnects, specifically where these aspects of construction relate to and can be compared with aspect of construction of the underlying interconnect metallization. The invention provides significantly improved methods of semiconductor device packaging by applying cost effective methods of packaging.

It is clear that metallization systems typically are created to provide functions such as power planes, signal lines and ground planes. What however is not implied in this is that metal lines that constitute the metallization system can be of

robust (wider than) construction, specifically when compared with underlying lines of interconnect metal. The top metallization system of the invention is for instance not limited to only providing ground planes but can, based on electrical design parameters and the possibilities and limitations that are imposed by these electrical design parameters, be extended to include other types of interconnect lines such as signal lines and power lines.

Claim 9 specifies that methods of the invention also allow for the creation of electrical contact points. In the creation of metal interconnect structures, the interconnects between overlying layers are in many application provided by contact vias are damascene structures. These methods of providing electrical contact points require specific method of processing, claim 9 is therefore included as part of the processes of the invention in view of the fact that electrical contact points can, using the methods of the invention, be provided concurrently with the creation of other lines of metal interconnect. The creation of contact points is part of the processes of the invention without requiring any special processing sequence others than the processing steps of the invention. Since electrical contact points can be created as part of the processes of the invention, these electrical contact

points need to be included in the claims of the invention. Claims 10 and 52 further emphasize this point by specifying the design range of the contact points that can be provided using the processes of the invention, making the size of the contact points that can be provided by using the processes of the invention be in accordance with the overall objectives of providing a novel way of packaging semiconductor devices.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 3-10 and 50-55 are objected to under 37 CFR 1.75 (c) as being improper dependent form for failing to further limit the subject matter of previous claim be withdrawn.

The specifications and drawings have been corrected as kindly suggested by Examiner, a copy of the updated drawings is attached.

In light of the above arguments, it is suggested that the Claims clearly distinguish the invention from the prior art. All claims are therefore believed to be in condition for allowance. Allowance of all claims is therefore respectfully requested.

It is requested that should Examiner Garcia not find the claims to be allowable that he call the undersigned Attorney at his convenience at 914-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

George O. Saile

George O. Saile (Reg. 19,572)